multiLane

ML4064-LB-112

Technical Reference

OSFP Electrical Passive Loopback Module

CMIS 3.0 Compliant

Innovation for the next generation

Table of Contents

ML4064-LB-112 OSFP 8x112G Passive Loopback Module - Key Features

- ✓ Loops back TX & RX with good performance SI Traces
- ✓ Built with advanced PCB Material
- ✓ MSA Compliant Shell with latching mechanism
- ✓ Nine thermal spots
- ✓ Can emulate all five OSFP power classes
- ✓ Can dissipate up to 17.4 W
- ✓ I2C Terminated by microcontroller, I2C slave compliant with MSA
- ✓ Implements MSA Memory Map with programmable new pages
- ✓ Ability to control/ monitor all low speed signals
- ✓ Two temperature sensors
- ✓ Insertion Counter
- ✓ Front LED Indicator
- ✓ Hot Pluggable
- ✓ Cut-off temperature preventing module overheating
- ✓ AC-coupled High Speed Interface

LED Indicator

Green (Solid) – Signifies that the module is operating in high power mode.
Red (Solid) – Signifies the module is operating in low power mode.
Green (Blinking) – Module in high power mode and Voltage or Temperature Alarm is triggered.
Red (Blinking) – Module in Low power mode and Voltage or Temperature Alarm is triggered.

Recommended Operating Conditions

Parameter	Symbol	Notes/Conditions	Min	Typ	Max	Units
Operating Temperature	T_A		0		85	°C
Supply Voltage	VCC	Main Supply Voltage	2.97	3.3	3.63	V
Input/output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω
Power Class		Programmable to Emulate all power classes	0		17.4	W
Data Rate	Rb	Guaranteed to work at 112Gbps per lane			800	Gbps

1. General Description

The ML4064-LB-112 is an OSFP passive electrical loopback module which is a hot pluggable form factor designed for high speed testing application for OSFP host ports. The ML4064-LB-112 is designed for 800 Gigabit Ethernet applications and provides 8x112G RX and TX lanes, I2C module management interface and all the OSFP SFF hardware signals.
The ML4064-LB-112 loops back 8-lane 112 Gbps transmit data from the Host back to 8-lane 112Gbps receive data port to the Host.
The ML4064-LB-112 provides programmable power dissipation up to 17.4 W allowing the module to emulate all the OSFP power classes. It also provides an insertion counter, a LED blinking rate, an upper temperature cut-off and a temperature sensor.

2. Functional Description

2.1 I2C Signals, Addressing and Frame Structure

2.1.1 I2C Frame

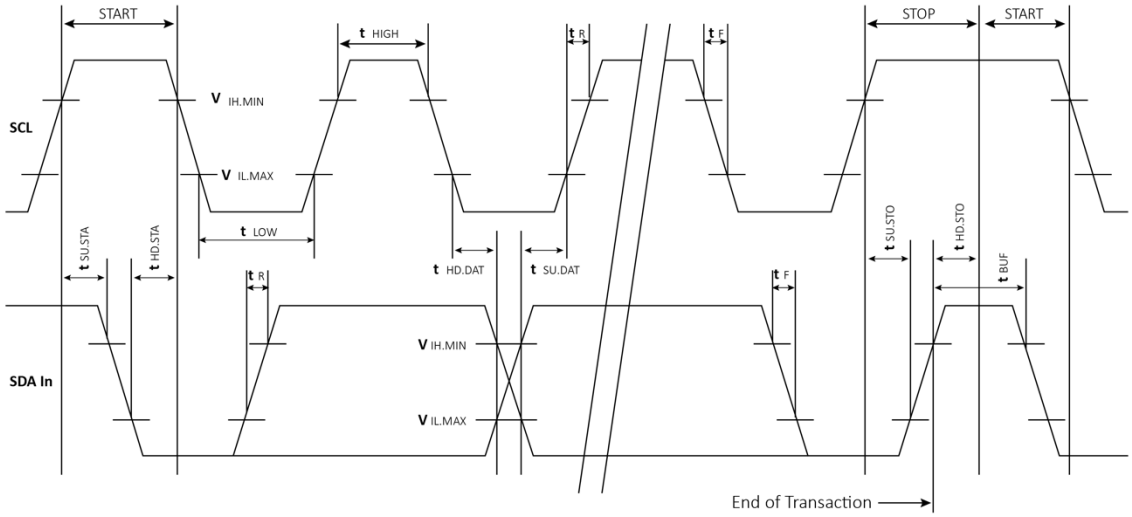


Figure 1: OSFP Timing Diagram

2.1.2 Management Timing Parameters

The timing parameters for the 2-Wire interface to the OSFP module are shown in the table below:

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f_{SCL}		400	kHz
Clock Pulse Width Low	t_{LOW}	1.2		us
Clock Pulse Width High	t_{High}	1.1		us

Time bus free before new transmission can start	t_{BUF}	20.8		us
Input Rise Time (400kHz)	$T_{R,400}$	300		Ns
Input Fall Time (400kHz)	$T_{F,400}$	300		ns
Serial Interface Clock HoldOff (Clock Stretching)	T_Clock_hold		500	us

Maximum time the OSFP Module may hold the SCL line low before continuing with a read or write operation is 500us.

2.1.3 Device Addressing and Operation

Serial Clock (SCL): The host supplied SCL input to OSFP transceivers is used to positive-edge clock data into each OSFP device and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain or open-collector driven.

Master/Slave: OSFP transceivers operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.

Device Address: Each OSFP is hard wired at the device address A0h.

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicating a START or STOP condition. All addresses and data words are serially transmitted to and from the OSFP in 8-bit words. Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one-bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host are acknowledged by OSFP transceivers. Read data bytes transmitted by OSFP transceivers should be acknowledged by the host for all but the final byte read, for which the host should respond with a STOP instead of an ACK.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the OSFP management interface can be reset. Memory reset is intended only to reset the OSFP transceiver management interface (to correct a hung bus). No other transceiver functionality is implied.

1. Clock up to 9 cycles

2. Look for SDA high in each cycle while SCL is high
3. Create a Start condition as SDA is high

Device Addressing: OSFP devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits in Figure 1. This is common to all OSFP devices.

1	0	1	0	0	0	0	R/W
MSB							LSB

Figure 1: OSFP Device Address

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address the OSFP transceiver output a zero (ACK) on the SDA line to acknowledge the address.

2.2 I2C Read/Write Functionality

2.2.1 OSFP Memory Address Counter (Read and Write Operations)

OSFP devices maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the module. This address stays valid between operations as long as OSFP power is maintained. The address "roll over" during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

2.2.2 Read Operations

A. Current Address Read

A current address read operation requires only the device address read word (10100001) be sent, see Figure 2 below.

		<--- CONTROL WORD --->																	
MASTER	START	MSB						LSB	READ									NACK	STOP
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
SLAVE										ACK	MSB							LSB		
											<---- DATA WORD ----->									

Figure 2: OSFP Current Address Read Operation

Once acknowledged by the OSFP, the current address data word is serially clocked out. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

B. Random Read

A random read operation requires a “dummy” write operation to load in the target byte address as shown in Figure 3 below. This is accomplished by the following sequence.

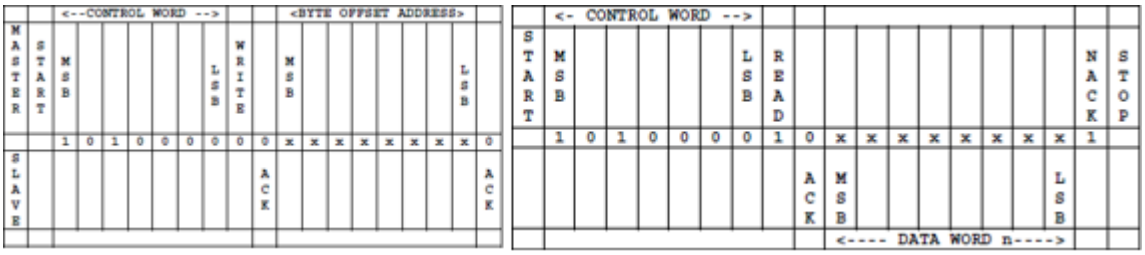


Figure 3: OSFP Random Read

The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the OSFP. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001). The OSFP acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

C. Sequential Read

Sequential reads are initiated by a current address read (Figure 4). To specify a sequential read, the host responds with an acknowledgement (instead of a STOP) after each data word. As long as the OSFP receives an acknowledgement, it will serially clock out sequential data words.
The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledgement.

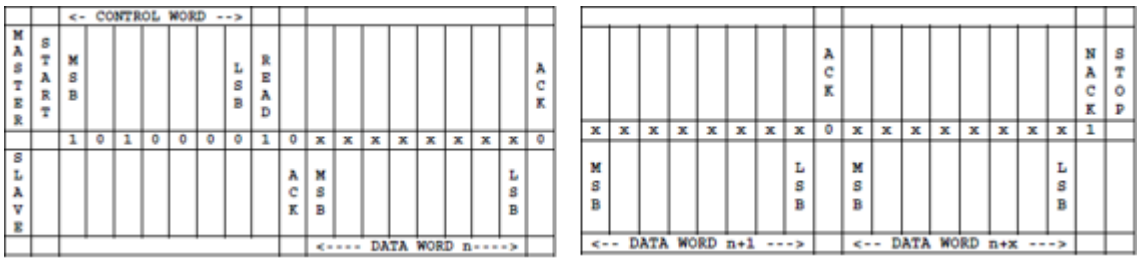


Figure 4: Sequential Address Read Starting at OSFP Current Address

2.3 Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status.

2.3.1 INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module.
Reset is an active low signal on the host which is translated to an active low signal on the module.
Interrupt is an active high signal on the module which gets translated to an active low signal on the host.

2.3.2 LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present.
Low Power mode is an active low signal on the host which gets converted to an active low signal on the module.
Module Present is controlled by a pull down resistor on the module which gets converted to an active low logic signal on the host.

2.4 ML4064-LB-112 Specific Functions

2.4.1 Voltage Sense

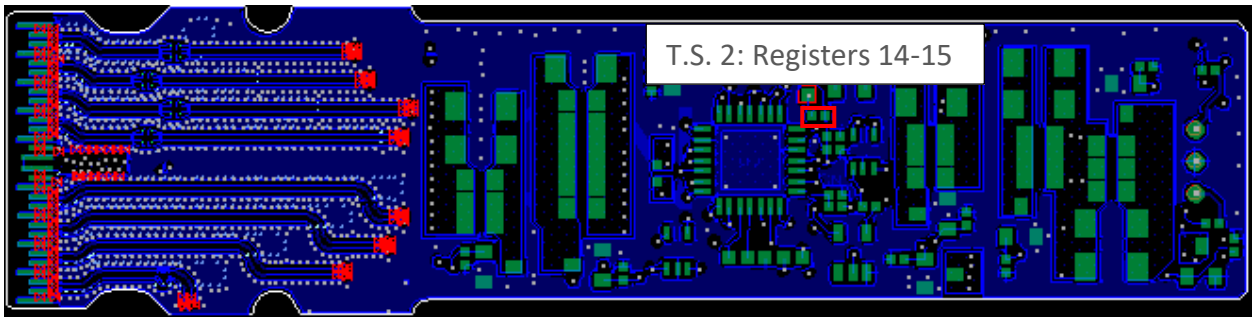
A voltage sense circuit is available allowing the measure of internal module supplied voltage Vcc. Supply voltage is represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value (0 – 65535) in increments of 100 µV, yielding a total measurement range of 0 to +6.55 Volts.

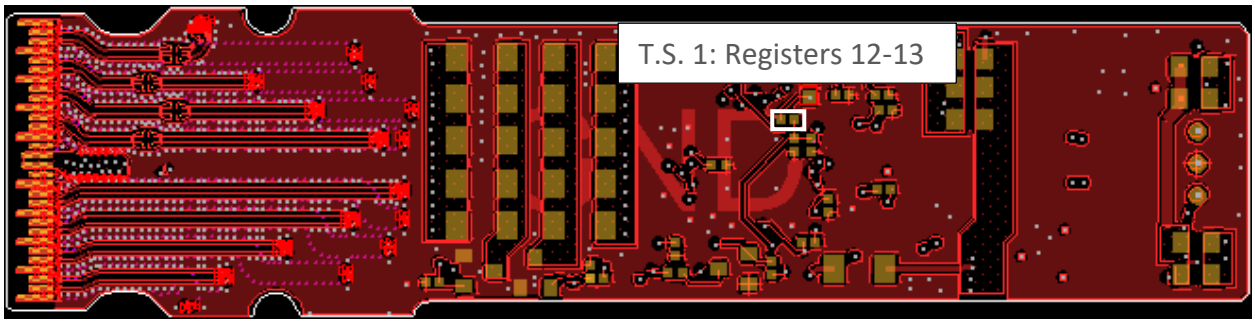
Address	Bit	Name	Description	Type
16	All	Supply voltage MSB	Internally measured supply voltage	RO
17	All	Supply voltage LSB	Internally measured supply voltage	

2.4.2 Temperature sense

The ML4064-LB-112 has two internal temperature sensors (top and bottom) in order to continuously monitor the module temperature. The temperature sensor values for top case readings are present in low-memory registers 14-15 and for the bottom are in registers 12-13. Internally measured Module temperature are represented as a 16-bit signed two's complement value in increments of 1/256 degrees Celsius. Temperature accuracy is better than ±1 degrees Celsius over specified operating temperature and voltage.

Address	Bit	Name	Description	Type
12 Lower page	All	Temperature 1 MSB	Internally measured TempSense1 (PCB Bottom)	RO
13 Lower page	All	Temperature 1 LSB	Internally measured TempSense1(PCB Bottom)	
14 Lower page	All	Temperature 2 MSB	Internally measured TempSense2 (PCB Top)	
15 Lower page	All	Temperature 2 LSB	Internally measured TempSense2 (PCB Top)	





2.4.3 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is pre-defined.
The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. Once the module temperature reaches the cut-off temperature, the PWM will automatically turn off in order to prevent overheating. Once the temperature is 5 degrees below cut-off value, the PWM goes back to its previous value.
The Cut-Off temperature for the ML4064-LB-112 is 85°C and it can be programmed to any value from register 253 of memory page 03. The Max Value that can be written is 90◦C.

Address	Bit	Name	Description	Type
253	7:0	Cut-Off temperature	Module Cut-Off Temperature, LSB = 1 degC	RW (NVR)

2.4.4 Programmable Power Disspation and Thermal Emulation

In upper **Page 00**, bit 0 of register 200 determines the power up of the module. The default value is 0 referring to Custom Power Mode. The power class identifier is selected when the value is 1.

Register	Page	Bit	Description	Default Value	Memory Type
200	Page 00h	0	Power Up Mode: Write 0b: Customer Power Mode Write 1b: Power Class Mode	0	RW

A. Custom Power Mode

The consumed power changes accordingly when the value of the power control registers changed (only when in high power mode). In Low power mode the module automatically turns off all power spots. In addition to the PWM controlled spots, there is static controlled power spots. The values written in these registers are permanently stored. The power spots can also be used for module thermal emulation. All registers are in upper page 03.

Register	Page	Bit	Control Type	Description	Default Value	Memory Type
251	Page 03h	7:0	PWM	PWM1 at the Bottom Controlled From 0 to 255	1.94 W	RW (NVR)
252		7:0		PWM2 at the Bottom Controlled From 0 to 255	1.45 W	
250		6	Static	PWM9 at the Bottom 0: disabled 1: enabled	1.45 W	
		5		PWM8 at the Bottom 0: disabled 1: enabled	1.8 W	
		4		PWM7 at the Top 0: disabled 1: enabled	1.94 W	
		3		PWM6 at the Top 0: disabled 1: enabled	1.94 W	
		2		PWM5 at the Top 0: disabled 1: enabled	1.94 W	
		1		PWM4 at the Top 0: disabled 1: enabled	3 W	
		0		PWM3 at the Top 0: disabled 1: enabled	1.94 W	

B. Power Class

The power class identifier specifies maximum power dissipation, when selecting a power class, the module operates at its maximum power.

Register	Page	Bit	Name	Description	Memory Type
200	Page 00h	7~5	Module Card Power Class	000: Power class 1 (2 W maximum) 001: Power class 2 (4 W maximum) 010: Power class 3 (8 W maximum) 011: Power class 4 (12 W maximum) 100: Power class 5 (16 W maximum)	RW
		4~1	Reserved		
		0	Power up Selection	0: Custom Power Mode 1: Power Class	

The power spots distribution is shown in the image below.

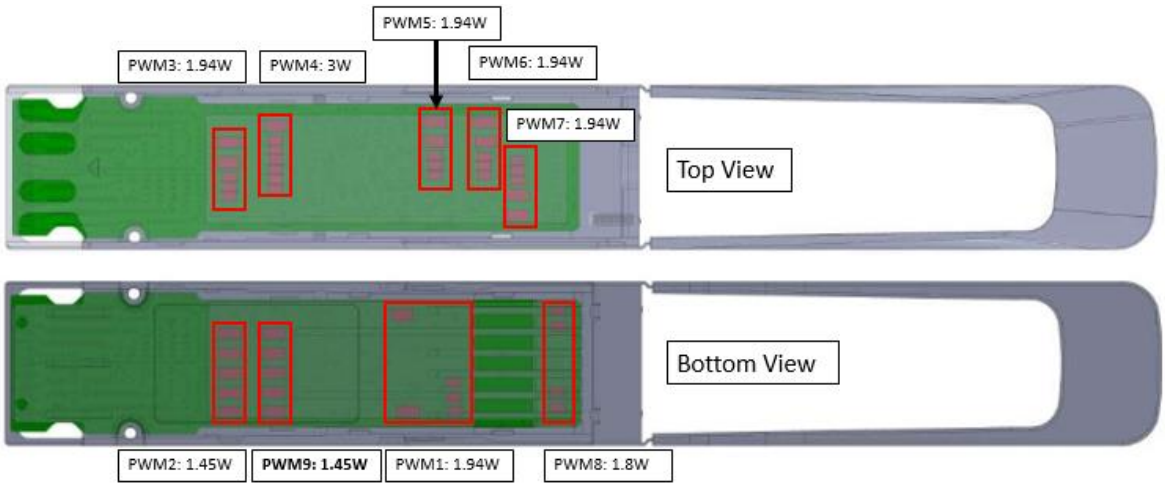


Figure 5: Power Spots Distribution

2.4.5 Low Speed Signals Pin Status

The register below is accessed from page 03h.

Register	Page	Bit	Name	Description	Memory Type
254	Page 03h	1	LPWn/PRSn	Read 1b: High Read 0b: Low	RO
		4	LPWn pin state transition	Read 0b: No edge detected Read 1b: Either rising edge or falling edge crossing the 1.25V threshold is detected Write 0b: No effect Write 1b: Clear the register	RW

2.4.6 IntL Control

During power-up of the module, INT is defaulted to negated. Afterward, host can set the status of this indicator to any status through an I2C registers **in upper page 03**. Setting it should not affect any operation in the module.

Address	Bit	Name	Description	Type
255	1~0	IntL_CNT	Digital Control of INTL: 00: Normal Operation 10: Force the INTL to logic 0 11: Force the INTL to logic 1	RW

For "Normal Operation", the INTL is asserted when the alarm or warning is high (VCC or Temperature) and the LED will start blinking. If the INTL_CNT is set from this register, the LED won't blink.

2.4.7 Insertion counter

The Insertion counter contains the number of times the module was plugged in a host. The insertion counter is incremented every time the module goes in initializing sequence, as it is nonvolatile it is always saved. The insertion counter can be read from registers 248 and 249 page03.

Address	Page	Name	Description	Type
248	Page 03h	Insertion Counter MSB		RO
249		Insertion Counter LSB	LSB unit = 1 insertion	

2.4.8 Maximum Power Indicator

The maximum power in the module is indicated by reading register 201 of Page 00. The value of this register is the maximum power consumption in multiples of 0.25 W rounded up to the next whole multiple of 0.25 W.

Address	Page	Bit	Name	Description	Default	Type
201	Page 00h	All	Max Power Indicator	**Module Maximum Power Consumption**	In decimal: 70 Corresponding to 17.4W	RO

2.4.9 Alarm and warning thresholds

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory-preset values allow the user to determine when a particular value is exceeding the predefined limit. While Voltage LSB unit is 100 µV and Temperature LSB unit is 1/256 ˚C.

Address	Page	Bit	Name	Default Value (DEC)	Default Value (HEX)	Type
128	Page 02h	ALL	high temp alarm threshold (MSB)	80°C	0x50	RW
129		ALL	high temp alarm threshold (LSB)		0x00	
130		ALL	low temp alarm threshold (MSB)	0° C	0x00	
131		ALL	low temp alarm threshold (LSB)		0x00	
132		ALL	high temp warning threshold (MSB)	75°C	0x4B	
133		ALL	high temp warning threshold (LSB)		0x00	
134		ALL	low temp warning threshold (MSB)	5°C	0x05	
135		ALL	low temp warning threshold (LSB)		0x00	
136		ALL	high volt alarm threshold (MSB)	3.63 V	0x8D	
137		ALL	high volt alarm threshold (LSB)		0xCC	
138		ALL	low volt alarm threshold (MSB)	2.97 V	0x74	
139		ALL	low volt alarm threshold (LSB)		0x04	
140		ALL	high volt warning threshold (MSB)	3.58 V	0x8B	
141		ALL	high volt warning threshold (LSB)		0xD8	
142		ALL	low volt warning threshold (MSB)	3.02 V	0x75	
143		ALL	low volt warning threshold (LSB)		0xF8	

3. High Speed Signals

High speed signals are electrically looped back from TX side to RX side of the module, all differential TX pairs are connected to the corresponding RX pairs, and the signals are AC coupled as specified by OSFP MSA High Speed Electrical specs.
The Passive traces connecting TX to RX pairs are designed to support a data rate up to 112Gbps.

4. OSFP Pin Allocation

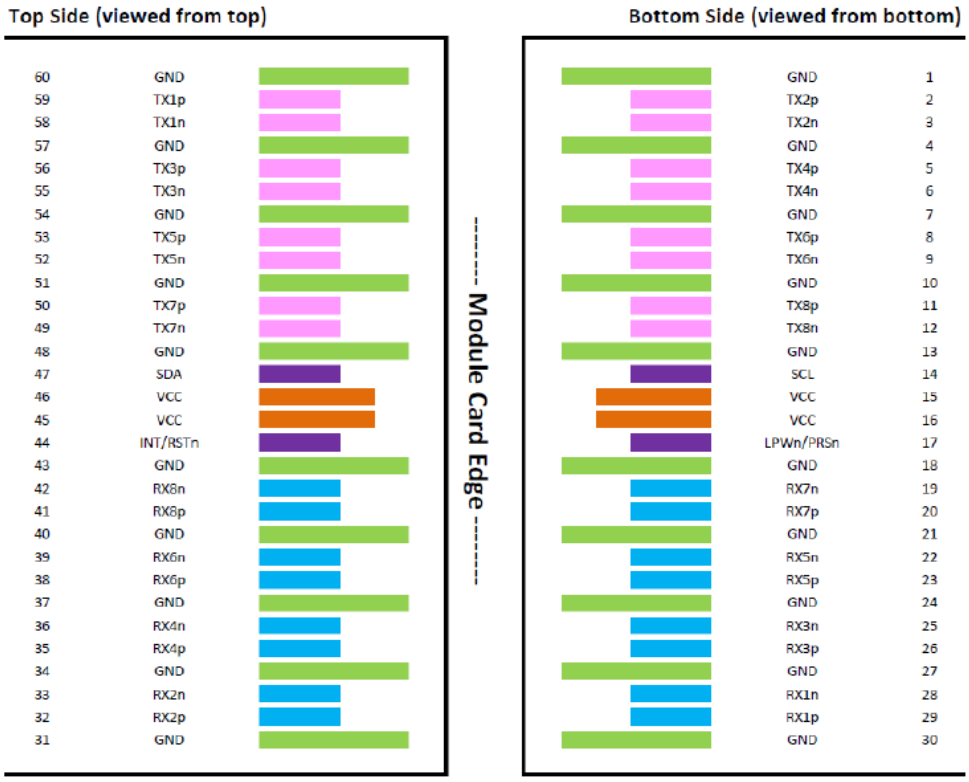


Figure 10: OSFP Module Pad Layout

Revision History

Revision number	Date	Description
0.1	9/21/2020	▪ Preliminary
0.2	1/15/2021	▪ Update section 2.4.2

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